Background and Motivation

- Neuroorphic Systems are brain inspired systems. They consist of neurons and synapses that process information.
- Online learning of synapses enables these systems to adapt. It is based on neuron spike timing.
- Memristors have been widely leveraged to construct synapses.\(^1\)
- Resistive switching of memristors plays a crucial role in the online learning of these synapses.
- Asymmetry in switching characteristics\(^2-4\) impacts learning in memristive synapses.

Twin-Memristor Synapse

- Consists of two memristors connected with opposite polarity.
- These memristors drive opposite currents, each depending on the memristance values.
- Synaptic weight dependent on effective conductance given by:

\[
G_{\text{eff}} = \frac{1}{M_p} - \frac{1}{M_n}
\]

Quad-Memristor Synapse

- Consists of four memristors. Two of them drive positive current while the other two drive negative current.
- Effective conductance is given by: \(G_{\text{eff}} = \frac{1}{M_1} + \frac{1}{M_2} - \frac{1}{M_3} - \frac{1}{M_4}\).
- While both devices switch and in opposite directions in the twin memristor synapse, only one of them switches here during learning and only in the LRS to HRS direction.
- Sensing phase determines which device switches in a future learning phase.
- A pair of memristors driving opposite currents and having equal memristance are both RESET to LRS.

Simulation Results

Twin-Memristor Synapse

Simulation results showing two a pre-synaptic neuron fire leading to the fire of a post-synaptic neuron. This leads to the potentiation of the synapse (weight increase).

Quad-Memristor Synapse

Simulation results showing two successive poteniations and three depressions of the synapse leading to the condition \(M_1 = M_2\). This leads to a RESET operation.

Comparison

The quad memristor synapse has higher silicon footprint, consumes more power and energy per spike and has an additional phase of operation.

<table>
<thead>
<tr>
<th>Metric</th>
<th>Twin Memristor</th>
<th>Quad Memristor</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of MOS devices</td>
<td>80</td>
<td>1481</td>
</tr>
<tr>
<td>No. of memristors</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>10 MHz</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Phases of Operation</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Average Power</td>
<td>45.35 (\mu)W</td>
<td>306.2 (\mu)W</td>
</tr>
<tr>
<td>Energy per Spike</td>
<td>4.558 (p)J</td>
<td>30.6 (p)J</td>
</tr>
</tbody>
</table>

Conclusions

- Although the twin memristor synapse is more efficient, it fails for drastically asymmetric switching times in memristors.
- Better device stacks must be made, reducing the asymmetry in switching times.
- Our quad memristor synapse can be used for highly asymmetric devices.

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References